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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,400	04/12/2004	German R. Gutierrez	BU1647C2	2892

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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,400	GUTIERREZ ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *1-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 4, filed January 21, 2009, with respect to 35 U.S.C. 112, first paragraph have been fully considered and are persuasive. The rejection of claim 3 has been withdrawn.

Claim Objections

2. Claims 1-8 are objected to because of the following informalities:

Claim 1, line 16, "an output signal" should be "the output signal" for clarity. See claim 1, line 1.

Claim 6, line 2, "the filtered signal" should be "the filtered detector signal".

The dependent claims 2-5 and 7-8 are objected to because they are either directly or indirectly depended on the objected independent claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laws et al. (U.S. Patent No. 4,943,788, hereinafter "Laws"), in view of Yabuki et al. (U.S. Patent No. 5,332,978, hereinafter "Yabuki"), Volk (U.S. Patent No. 5,384,502), and Everitt et al. (U.S. Patent No. 6,188,739, hereinafter "Everitt").

Laws discloses a receiver shown in Fig. 1 comprising two phase locked loop (PLL) circuits and a mode select logic 24 for receiving an incoming data RCVD and a reference clock signal LSCK. A first PLL circuit comprises a phase detector 10, a linear multiplexer 16, a loop filter 18, and a VCO 14. A second PLL circuit comprises a phase and frequency comparator or detector 20, the linear multiplexer 16, the loop filter 18, the VCO 14, and a frequency divider 22. The phase error signal from the comparator 20 is applied to the VCO 14 via the linear multiplexer 16, which is operative to select the inputs from the detector 10 and the comparator 20 under the control of the mode select logic 24. Also see col. 2, lines 27-53.

Regarding claim 1, clearly, Laws disclose all the claimed subject matters, except, Laws does not explicitly show, teach, or suggest there is a charge pump coupled between the detector 10 and the multiplexer 16 in the first PLL circuit, and a low pass filter and a GM amplifier coupled with the comparator 20 and the multiplexer 16.

Yabuki discloses multiple embodiments of frequency synthesizers. Fig. 1 shows one of the frequency synthesizers comprising three PLL circuits. Referring to Fig. 1, a switch or multiplexer 22 is coupled to a first PLL circuit 9 and a third PLL circuit 21 for selecting one of the output signals of the phase detectors 6 and 19 through charge pumps 7 and 20, respectively. Clearly, the charge pump 7 or 20 is coupled between the phase detector 6 or 19 and the switch 22.

Volk discloses a PLL circuit 60 in Fig. 3 comprising a phase comparison circuit 61, which receives an external data input signal Θ_D and a reference signal Θ_{FB} to generate a phase detected output signal (PD and/or UP) indicative of a phase difference between the input signal and the reference signal; a split loop filter 63 which filters the phase detected output signal through a charge pump 62 to provide a filtered output signal; a trans-conductance (gm) amplifier 64 which amplifies the filtered output signal to generate a current output signal I_{OS}; a variable gain current source 65 which receives the current output signal I_{OS} and a first current output signal I_{OS1} to generate a second current output signal I_{OS2}; a VCO 66 which receives the second current output signal I_{OS2} to generate an oscillator signal; and a frequency divider 67 which divides the frequency of the oscillator signal to generate the reference signal.

However, Volk fails to show, teach or suggest that a second filter is used coupled between the trans-conductance (gm) amplifier 64 and the VCO 66 to further filter the current output signal I_{OS} from the trans-conductance (gm) amplifier 64 before controlling the oscillator signal of the VCO 66.

Everitt also discloses a PLL circuit 400 in Fig. 4 comprising similar circuitries of Volk's PLL circuit. Further, the PLL circuit 400 also includes a second integrator (second filter) 450 coupled between a charge pump (sometime also called trans-conductance (gm) amplifier) and a signal controlled oscillator (VCO) 416 to generate a current signal to the VCO 416 in order to generate a reference signal to the phase or frequency comparator circuit 404. Also see col. 4, line 39 to col. 5, line 18.

Therefore, it would have been obvious to one of ordinary skill in the art that a general PLL circuit, such as Laws' second PLL circuit is capable of including a charge pump between the comparator 20 and the multiplexer 16 as taught by Yabuki in order to processing the integration of the phase difference of the comparator 20 prior generating a feedback clock signal provided by the loop filter 18 and the VCO 14. It is also obvious to one of ordinary skill in the art to include a low pass filter and a GM amplifier coupled with the phase detector 10 and the multiplexer 16 in Laws' first PLL circuit as taught by Volk and Everitt for the purpose of further or additionally filtering, for example, the current signal of the trans-conductance (gm) amplifier 64 prior controlling the frequency by the VCO 14.

Regarding claim 2, the split loop filter 63 shown in Fig. 4 of Volk's PLL circuit is indicated as a single-pole RC filter.

Regarding claim 3, the frequency divider 22 of Laws' second PLL circuit is coupled to the VCO 14 and divided the oscillator signal of the VCO 14 to generate the reference signal to the phase and frequency comparator 20.

Regarding claim 4, the incoming data RCVD is a serial data stream.

Regarding claim 5, it is well known to an artisan to know that the incoming data RCVD could be operated at a data rate of at least 2.488 Ghz if Laws' receiver circuit is used in a SONET OC-48 transceiver as pointed out at least in the Background of the Invention of the instant application on page 3, lines 8-12.

Regarding claim 8, the reference clock signal used in the comparator 20 10 is a reference clock signal generated by the VCO 14 through the frequency divider 22.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Laws in view of Yabuki, Volk, and Everitt as applied to claim 1 above, and further in view of Voorman (U.S. Patent No. 4,780,690).

Regarding claim 6, although Volk discloses that the trans-conductance (gm) amplifier 64 shown in Fig. 4 comprises amplifiers receiving the filtered signal of the split loop filter 63 and a current load circuit coupled to the amplifiers to provide the current signal $I_{OS,}$ Volk does not explicitly show, teach or suggest that the amplifiers are differential amplifiers.

Voorman is related to a filter arrangement having a trans-conductance circuit shown in Fig. 1. Fig. 3 shows a detailed block diagram of the trans-conductance circuit of Fig. 1. Referring to Fig. 3, the trans-conductance circuit comprises two differential amplifiers, which receive the filtered signal of the filter arrangement of Fig. 1 and a

current load circuit I_5 coupled to the differential amplifiers to provide a current signal. Also see col. 5, lines 1-24.

Therefore, it would have been obvious to one of ordinary skill in the art that Volk's trans-conductance (gm) amplifier 64 which could be implemented in Laws' first PLL circuit is capable of or being integrated by a differential amplifier and a current load circuit as taught by Voorman in order to generate a current signal from a current of a filter.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Laws in view of Yabuki, Volk, and Everitt as applied to claim 1 above, and further in view of Hotine (U.S. Patent No. 4,656,647).

Regarding claim 7, although Laws does not explicitly show, teach or suggest that the output signal of the phase detector 10 of the first PLL circuit has a peak to peak signal swing of less than one volt.

Hotine also discloses a PLL circuit in Fig. 2 comprising a phase comparator 45, a low pass filter 48 and a VCO 50, wherein the phase comparator 45 compares a voltage output signal 42 having a 0.2 peak to peak voltage through a squaring amplifier 43 with an oscillator voltage generated from the VCO 50. Obviously, the voltage at the output signal 47 of the phase comparator 45 has a peak to peak signal of less than one volt. Also see col. 8, line 45 to col. 9, line 25.

Therefore, it would have been obvious to one of ordinary skill in the art as taught by Hotine that Laws' phase detector 10 of the first PLL circuit is capable of generating a

voltage swing, for example, has a peak to peak signal of less than one volt in order to reduce the voltage of a voltage supply of the first PLL circuit.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is 571- 272-3051. The examiner can normally be reached on Monday-Friday 10:00-6:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on 571- 272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/YOUNG T. TSE/
Primary Examiner, Art Unit 2611